REMARKS

Claims 1-20 are pending. Reconsideration and allowance of all pending claims is respectfully requested in view of the following remarks.

Claim Rejections Under 35 U.S.C. §102

Claims 1-6, 8, 10-16, 18, and 20 are rejected under 35 U.S.C. §102 (b) over U.S. Patent 6,317,763 to Vatinel (hereafter Vatinel). This rejection is respectfully traversed.

Vatinel is directed to circuits, barrel shifters, and methods for manipulating a bit pattern. However, Vatinel does not disclose or suggest "each data input line has a one-to-one correlation to a single data transistor; ... all of the plurality of logic gates share a single data transistor for each data input" as recited in claim 1.

The Examiner asserts, on pages 2 and 3 of the Office Action, that Vatinel discloses that "each data input line has a one to one correlation to a single data transistor (each input data is connecting to a buffer as seen in part 6 of Figure 1 wherein the buffer is inherently comprised transistors); ... wherein all of the plurality of logic gates share a single data transistor for each data input (all the parts of row logic gates is are connected to the output of input data buffer)." Applicant respectfully disagrees. Referring to Figure 1 of Vatinel, each data input is inputted into nine p-feds in parallel. Therefore, the circuit shown in Figure 1 does not provide for one to one correlation between a data input line and a single data transistor. Furthermore, the circuit shown in Figure 1 does not share data transistors. Vatinel merely discloses, at column 1, lines 18-44, a standard barrel shifter that shifts and rotates the contents of a data path of an integrated circuit. A standard barrel shifter does not provide for data transistor sharing. Similarly, connecting all of the parts of row logic gates to the output of input data buffer does not teach or suggest that all of the logic gates share a single data transistor for each data input. Vatinel simply does not teach or suggest transistor level data sharing.

The logic circuit for use in a multiplexer as recited in claim 1 uses data sharing among transistors in order to reduces the number of transistors required by each logic gate. Referring to page, lines 12-16 of the specification, "instead of using a separate transistor for each input data line to each logic gate, only a single transistor is required in this example for a particular data input. The other data inputs are received from adjacent or other logic gates using shared data lines." Vatinel does not disclose or suggest the feature of enabling all of the logic gates to share a data transistor for each data input. Therefore, claim 1 is allowable.

Claims 2-6, 8, and 10 are allowable because they depend from allowable claim 1 and for the additional features they recite.

Regarding claim 11, for at least the same reason as noted above with respect to claim 1, Vatinel does not disclose or suggest "each data input line has a one-to-one correlation to a single data transistor; ... all of the plurality of logic gates share a single data transistor for each data input" as recited in claim 11. Therefore, claim 11 is allowable.

Claims 12-16, 18, and 20 are allowable because they depend from allowable claim 11 and for the additional features they recite. Withdrawal of the rejection of claims 1-6, 8, 10-16, 18, and 20 under 35 U.S.C. §102 (b) is respectfully requested.

Claim Rejections Under 35 U.S.C. §103

Claims 7 and 17 are rejected under 35 U.S.C. §103 (a) over Vatinel in view of U.S. Patent 5,961,575 to Hervin et al. (hereafter Hervin). This rejection is respectfully traversed.

Claims 7 and 17 are allowable because they depend from allowable claims 1 and 11, respectively, and for the additional features they recite. Withdrawal of the rejection of claims 7 and 17 under 35 U.S.C. §103 (a) is respectfully requested.

Claims 9 and 19 are rejected under 35 U.S.C. §103 (a) over Vatinel. This rejection is respectfully traversed.

Claims 9 and 19 are allowable because they depend from allowable claims 1 and 11, respectively, and for the additional features they recite. Withdrawal of the rejection of claims 9 and 19 under 35 U.S.C. §103 (a) is respectfully requested.

In view of the above remarks, Applicant respectfully submits that the application is in condition for allowance. Prompt examination and allowance are respectfully requested.

Should the Examiner believe that anything further is desired in order to place the application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

Date: **September 16, 2003**

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